# Buck Converter Load Regulation & Ripple Test

Project: PSU-BUCK5V3A-01 Load Regulation

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# Buck Converter Load Regulation & Ripple Test

This protocol verifies the output voltage stability and ripple performance of a 5 V / 3 A synchronous buck converter module across its full rated load range. It doubles as a template -
duplicate this file for the next board revision and swap in new equipment/data as needed.

## 1. Test Setup

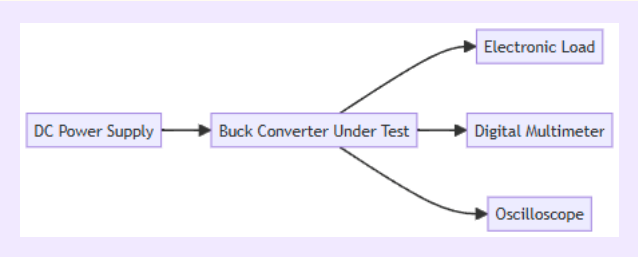



*Fig. 1*

Fig. 1 shows the measurement chain: a regulated 12 V bench supply feeds the converter under
test, whose output is simultaneously monitored by a DMM (steady-state voltage) and an oscilloscope
(ripple/noise), while a programmable electronic load sweeps the output current.

| Instrument | Model | Function |
|---|---|---|
| DC Power Supply | Rigol DP832A | Input source, CH1 set to fixed 12.0 V (30 V/3 A output) |
| Electronic Load | Rigol DL3021A | Programmable constant-current load, 150 V/40 A/200 W |
| Digital Multimeter | Rigol DM3058E | Output voltage measurement, 5½-digit |
| Oscilloscope | Rigol DHO4404 | Output ripple/noise measurement, 400 MHz, 4 GSa/s |

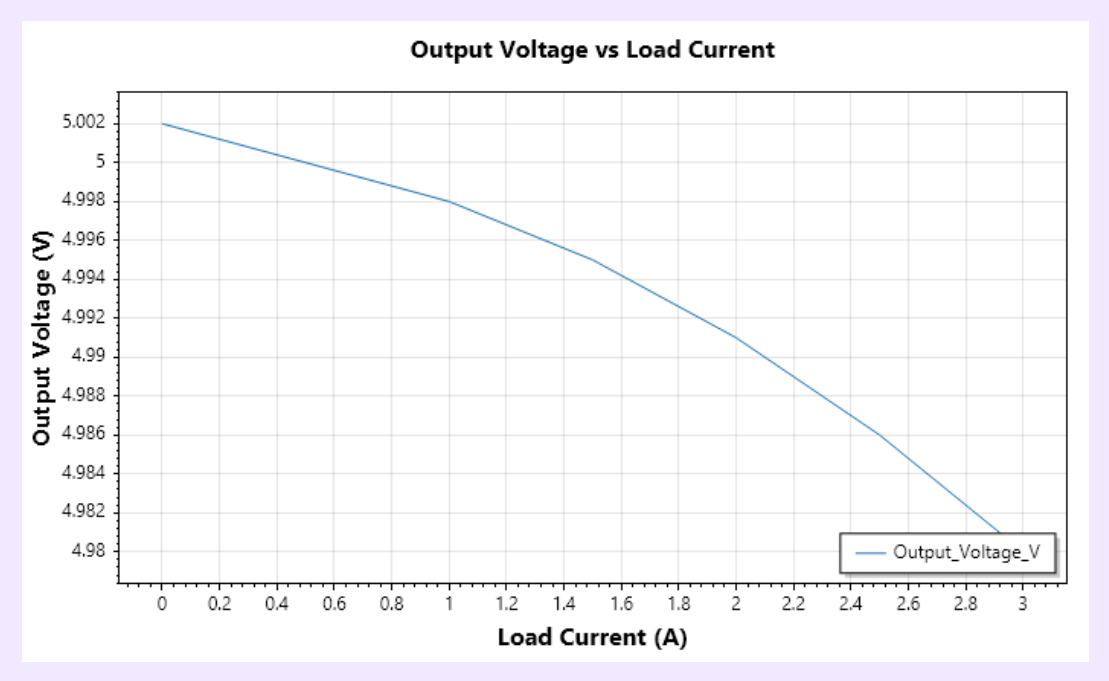
> **WARNING**
> The electronic load dissipates up to 15 W at full current - allow it to cool between runs and
> never exceed its rated input voltage. Confirm the converter's current-limit/thermal-shutdown
> behavior before the first run of a new board revision.

## 2. Procedure

1. Power the converter from the 12 V supply with the electronic load set to 0 A (no load).
2. Allow the output to settle for 60 s, then record the no-load output voltage.
3. Step the electronic load from 0 A to 3.0 A in 0.5 A increments.
4. At each step, wait 10 s for thermal/loop settling, then record output voltage (DMM) and peak-to-peak ripple (oscilloscope, 20 MHz bandwidth limit, AC-coupled).

> **NOTE**
> Zero the oscilloscope probe and verify DMM calibration before the first measurement - see the
> lab's standard calibration procedure[1].

# 3. Load Regulation



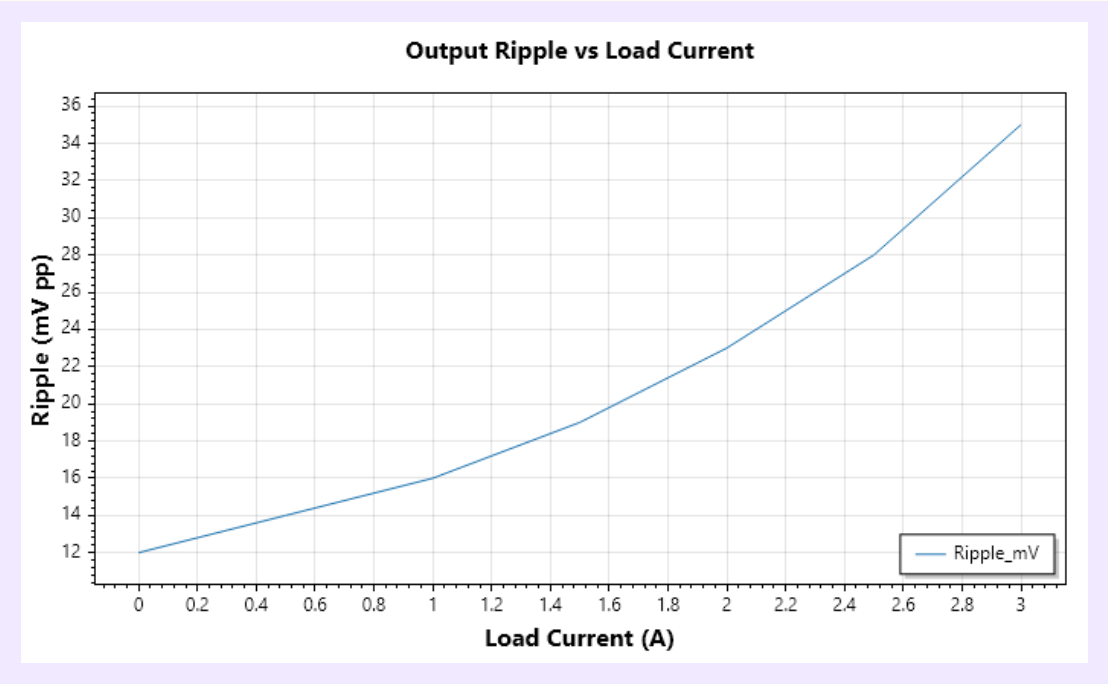

Load regulation is calculated per Eq. 1, using the no-load and full-load (3.0 A) readings from the chart above:

$$\text{Load Reg.} = \frac{V_{NL} - V_{FL}}{V_{NOM}} \times 100\%$$

*Eq. 1*

Where $V_{NL}$ is the no-load output voltage, $V_{FL}$ is the full-load output voltage, and $V_{NOM}$ is the nominal 5.0 V output. With $V_{NL}$ = 5.002 V and $V_{FL}$ = 4.980 V, this gives 0.44% - well within the ±1% design target.

# 4. Output Ripple




Ripple increases with load current as expected (higher switching currents through the output
inductor's ESR), but stays well under the 50 mV design limit across the full range.

# 5. Test Summary

| Test | Spec | Measured | Status |
|---|---|---|---|
| Output voltage (no load) | 5.00 V ± 2% | 5.002 V | PASS |
| Load regulation (0 → 3.0 A) | < 1% | 0.44% | PASS |
| Output ripple (full load) | < 50 mV pp | 35 mV pp | PASS |

*Table 1: Load regulation test results*

> **IMPORTANT**
>
> All results in Table 1 PASS against the design spec. Re-run this full procedure after any firmware, layout, or BOM change to the converter - a previous board revision passed load regulation but failed ripple after an inductor substitution.

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**Footnotes**

1. Internal calibration procedure QA-CAL-014, valid instrument calibration certificates required within the last 12 months.