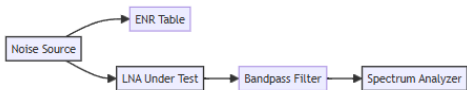




RF Low Noise Amplifier (LNA) Test Report

1. Test Setup Architecture

The following block diagram illustrates the hardware pipeline for evaluating the LNA gain (S21) and noise figure (NF). The setup uses a calibrated noise source and a spectrum analyzer with a noise figure measurement personality.



WARNING

Maximum continuous input power to the Spectrum Analyzer RF port must not exceed +10 dBm to prevent front-end saturation and permanent mixer damage.

2. Theoretical Cascaded Noise Figure

When cascading the LNA with the measurement equipment, the total system noise figure is calculated using the Friis formula. To isolate the LNA performance, we must de-embed the spectrum analyzer's noise floor.

The total noise factor F_{total} is defined as:

$$F_{total} = F_{LNA} + \frac{F_{SA} - 1}{G_{LNA}}$$

Where:

- F_{LNA} is the noise factor of the amplifier under test (linear).
- F_{SA} is the noise factor of the spectrum analyzer (linear).
- G_{LNA} is the linear gain of the amplifier.

3. Swept Measurement Results

The table below summarizes the measured Gain and Noise Figure across the target 2.4 GHz ISM band. Data is averaged over 100 sweeps with a resolution bandwidth (RBW) of 1 MHz.

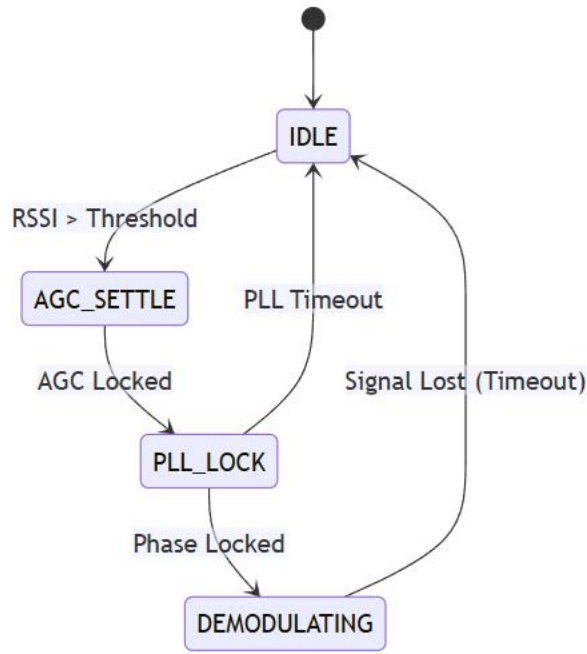
Frequency (GHz)	S21 Gain (dB)	Noise Figure (dB)	Test Status
2.400	18.2	1.15	PASS
2.425	18.4	1.12	PASS
2.450	18.5	1.10	PASS
2.475	18.3	1.14	PASS
2.500	17.9	1.21	PASS



Digital Demodulator: Firmware State Machine

1. State Machine Overview

The signal acquisition and tracking logic for the digital QPSK demodulator is implemented as a finite state machine (FSM). This logic runs in the primary DSP thread.



2. NCO Tuning Word Calculation

The Numerically Controlled Oscillator (NCO) frequency f_{out} is determined by the 32-bit Phase Accumulator width and the system clock f_{clk} . The Tuning Word (TW) is calculated as follows:

$$TW = \text{round}\left(\frac{f_{out} \cdot 2^{32}}{f_{clk}}\right)$$

For a system clock of 122.88 MHz and a target IF of 10.7 MHz, the firmware calculates and updates this tuning word dynamically within the PLL loop filter constraint.



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3. Baseband Register Map

Register Name	Address	Width	Access	Description
DSP_CTRL	0x0000	32-bit	R/W	DSP core control bits (Enable, Reset)
FSM_STATUS	0x0004	32-bit	R/O	FSM current state and lock flags
NCO_TW_REG	0x0010	32-bit	R/W	Phase accumulator tuning word
AGC_GAIN	0x0014	32-bit	R/O	Current variable gain amplifier state